

Appl. No. : 09/124,823  
Filed : July 29, 1998

10. (amended) The microprocessor integrated circuit of claim 8 further including memory controller means coupled to said memory for performing direct memory access data transfer through said one or more interface ports.

11. (amended) A microprocessor computational system comprising:  
a first processing unit disposed upon a first substrate;  
a first memory disposed upon said first substrate and coupled to said first processing unit, said first memory occupying a greater area of said first substrate than said first processing unit, said memory further occupying a majority of a total area of said substrate;  
a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said first substrate; and  
a second processing unit coupled to said first processing unit and configured for interprocessor communication with said first processing unit.

12. (amended) The microprocessor computational system of claim 11 wherein said second processing unit and a second memory are disposed upon a second substrate, said second memory occupying a greater area of said second substrate than said second processing unit said second memory further occupying a majority of a total area of said substrate.

13. (amended) The multiprocessor computational system of claim 11 wherein said first processing unit includes an interface port for establishing said interprocessor communication between an internal register of said first processing unit and second processing unit.

#### REMARKS

The specific changes to the amended title and claims are shown on a separate set of pages attached hereto and entitled **VERSION WITH MARKINGS TO SHOW CHANGES MADE**, which follows the signature page of this Amendment. On this set of pages, the insertions are underlined while the [deletions are in brackets and bolded].

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#### Discussion of the Title

The Applicant has amended the title to more clearly indicate the invention to which the claims are directed.

#### Discussion of the Specification

The Applicant has amended the Specification to insert, immediately following the title, a statement indicating that the present application is a continuation of a prior application. The statement also indicates the parent application has issued as a U.S. patent. The statement identifies the prior application as Application No. 08/484,918, filed June 7, 1995, which is now U.S. Patent No. 5,809,336.

#### Discussion of the Abstract

The Applicant has canceled the abstract provided in the Preliminary Amendment, dated July 29, 1998 and has presented a new abstract on a separate sheet, apart from any other text.

#### Status of the Claims

Claims 1-13 are pending in the application and are presented for examination.

#### Discussion of Rejections Under 35 USC §112

Claims 2-3, 5-7, 9-10, and 12-13 have been rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention.

The Applicant has amended Claims 2-3, 5-7, 9-10, and 12-13 to overcome the rejection. In particular, Claims 2-3 have been amended to depend from Claim 1. Claims 5-7 have been amended to depend from Claim 4. Claims 9-10 have been amended to depend from Claim 8. Claims 12-13 have been amended to depend from Claim 11. Thus, the Applicant has amended Claims 2-3, 5-7, 9-10, and 12-13 to depend from base claims that are present in the application.

#### Discussion of Rejections Under 35 USC §103

Claims 1, 4, and 8 have been rejected under 35 USC 103(a) as allegedly being unpatentable over Edwards et al. (US 4,680,698, hereinafter Edwards). In order for the

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Applicant's claims to be unpatentable over the prior art references, the prior art references must teach or suggest all of the claim limitations. The Office Action states that Edwards discloses a microprocessor integrated circuit comprising a processor and a memory being on the same substrate.

The Applicant has amended Claims 1, 4 and 8 to include the feature that a variable speed system clock is further disposed on the substrate. Support for the variable frequency ring oscillator is found in Applicant's specification, as filed, on page 4 at lines 15-20 and at page 24 line 31 through page 25 line 11. Edwards does not disclose the feature of a system clock on the same substrate as the processing unit. Edwards discloses in Figure 1 the structure of the microprocessor. The figure, as well as the accompanying description on Column 4 line 54 through Column 5 line 6, describe the clock as an external signal provided to the processor. Thus, Edwards fails to disclose at least one element of Applicant's Claims 1, 4, and 8, as amended. In view of the above, Applicant respectfully requests allowance of Claims 1, 4, and 8.

Claim 11 has also been rejected under 35 USC 103(a) as allegedly unpatentable over Edwards in view of Bell et al. (US 5,379,438, hereinafter Bell). The Applicant has amended Claim 11 to include a variable output frequency ring oscillator. The Applicant has also amended Claim 11 to include the feature that the first processing unit, first memory, and variable output frequency ring oscillator are disposed on a single substrate. As discussed above, Edwards does not disclose an oscillator on the same substrate as a processing unit. Bell also does not disclose a variable output frequency ring oscillator disposed on the same substrate as the first processing unit. Thus, neither Edwards nor Bell, either alone or in combination, disclose all features claimed in Applicant's Claim 11. Thus, the Applicant respectfully requests the allowance of Claim 11.

Claims 2-3, 5-7, 9-10, and 12-13 depend from one of Claims 1, 4, 8, or 11 and are believed to be allowable as depending from an allowable base claim. Accordingly, Applicant respectfully requests the allowance of Claims 2-3, 5-7, 9-10, and 12-13.

### CONCLUSION

The Applicant has amended the Claims to overcome all of the rejections detailed in the Office Action dated January 31, 2000. The Applicant thus respectfully requests allowance of all outstanding claims. The Applicant has endeavored to address all of the concerns as expressed in

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the Office Action. Accordingly, amendments to the claims, the reasons therefor, and arguments in support of patentability of the pending claim set are presented above. Any claim amendments which are not specifically discussed in the above remarks are made in order to improve the clarity of claim language, to correct grammatical mistakes or ambiguities, and to otherwise improve the clarity of the claims to particularly and distinctly point out the invention to those of skill in the art. Finally, the Applicant submits that the claim limitations discussed above represent only illustrative distinctions. Hence, there may be other patentable features that distinguish the claimed invention from the prior art.

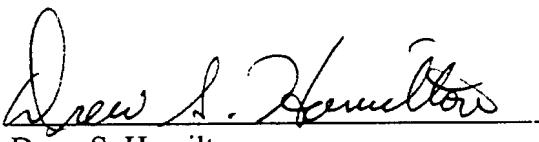
If the Examiner finds any remaining impediment to the prompt allowance of these claims that could be clarified with a telephone conference, the Examiner is respectfully requested to initiate the same with the undersigned.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

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Dated: April 29, 2002

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VERSION WITH MARKINGS TO SHOW CHANGES

IN THE TITLE

[HIGH PERFORMANCE, LOW COST MICROPROCESSOR] HIGH PERFORMANCE  
MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK

IN THE CLAIMS

1. (amended) A microprocessor integrated circuit comprising:  
a program-controlled processing unit operative in accordance with a sequence of program  
instructions;

a memory coupled to said processing unit and capable of storing information provided by  
said processing unit;

a plurality of column latches coupled to the processing unit and the memory, wherein,  
during a read operation, a row of bits are read from the memory and stored in the column latch;  
and

a variable speed system clock having an output coupled to said processing unit;  
said processing unit, said variable speed system clock, said plurality of column latches,  
and said memory fabricated on a single substrate, said memory using a greater area of said single  
substrate than said processing unit, said memory further using a majority of a total area of said  
single substrate.

2. (amended) The microprocessor integrated circuit of claim [7]1 wherein said memory  
is dynamic random-access memory.

3. (amended) The microprocessor integrated circuit of claim [7]1 wherein said memory  
is static random-access memory.

4. (amended) A microprocessor integrated circuit comprising:  
a processing unit disposed upon an integrated circuit substrate, said processing unit  
operating in accordance with a predefined sequence of program instructions; [and]  
a memory coupled to said processing unit and capable of storing information provided by  
said processing unit, said memory occupying a larger area of said integrated circuit substrate than

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said processing unit said memory further occupying a majority of a total area of said single substrate; and

a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said integrated circuit substrate.

5. (amended) The microprocessor integrated circuit of claim [7]4 wherein said memory is dynamic random-access memory.

6. (amended) The microprocessor integrated circuit of claim [7]4 wherein said memory is static random-access memory.

7. (amended) The microprocessor integrated circuit of claim [7]4 wherein said memory is capable of supporting read and write operations.

8. (amended) A microprocessor integrated circuit comprising:  
a processing unit having one or more interface ports for interprocessor communication, said processing unit being disposed on a single substrate; **[and]**  
a memory disposed upon said substrate and coupled to said processing unit, said memory occupying a greater area of said substrate than said processing unit, said memory further comprising a majority of a total area of said substrate; and  
a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said substrate.

9. (amended) The microprocessor integrated circuit of claim [7]8 wherein a first of said interface ports includes a column latch, said column latch facilitating serial communication through said first of said interface ports.

10. (amended) The microprocessor integrated circuit of claim [7]8 further including memory controller means coupled to said memory for performing direct memory access data transfer through said one or more interface ports.

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11. (amended) A microprocessor computational system comprising:  
a first processing unit disposed upon a first substrate;  
[ and] a first memory disposed upon [a] said first substrate and coupled to said first processing unit, said first memory occupying a greater area of said first substrate than said first processing unit, said memory further occupying a majority of a total area of said substrate;  
a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said first substrate; and  
a second processing unit coupled to said first processing unit and configured for interprocessor communication with said first processing unit.

12. (amended) The microprocessor computational system of claim 11 [81] wherein said second processing unit and a second memory are disposed upon a second substrate, said second memory occupying a greater area of said second substrate than said second processing unit said second memory further occupying a majority of a total area of said substrate.

13. (amended) The multiprocessor computational system of claim 11 [81] wherein said first processing unit includes an interface port for establishing said interprocessor communication between an internal register of said first processing unit and second processing unit.

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## HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK

### Abstract of the Disclosure

A microprocessor integrated circuit including a processing unit disposed upon an integrated circuit substrate is disclosed herein. The processing unit is designed to operate in accordance with a predefined sequence of program instructions stored within an instruction register. A memory, capable of storing information provided by the processing unit and occupying a larger area of the integrated circuit substrate than the processing unit, is also provided within the microprocessor integrated circuit. The memory may be implemented using, for example dynamic or static random-access memory. A variable output frequency system clock, such as generated by a ring oscillator, is also disposed on the integrated circuit substrate.